PVP 20

Code: 20EC3302

II B.Tech - I Semester – Regular Examinations - FEBRUARY 2022

DIGITAL LOGIC DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

UNIT – I

1. a) What are the canonical and standard forms of a Boolean function? Explain with an example. 7 M

   b) Solve the following

      i) $(57.125)_{10} = (\ )_8$

      ii) $(30.6875)_{10} = (\ )_2$

      iii) $(137.75)_8 = (\ )_{10}$ 7 M

OR

2. a) Reduce the following Boolean expressions.

      i) AB+A(B+C)+B(B+C)

      ii) ABEF+ AB(EF)′+(AB)′EF.

      iii) A′B′+A′BC′+A′BCD+A′BC′D′E. 7 M

   b) Perform the given subtraction using 1's and 2's complement methods: $(10110)_2$ - $(1101101)_2$. 7 M

UNIT – II

3. a) Obtain the simplified expression in sum of products and product of sums form using K-map method.
   F(A,B,C,D,E) = ∑(0,1,4,5,9,16,17,21,25,29)
   7 M

b) Obtain minimal POS expression for the Boolean function.
$F(A,B,C,D) = \Pi(0,1,2,3,4,6,9,10)+d(7,11,13,15)$.
Draw the circuit using 2 input NAND gates. 7 M

OR

4. a) Draw NOR logic diagram that implements the following function.
$F(A,B,C,D) = \Pi(0,1,2,3,4,8,9,12)$ 7 M

b) Realize logic gates AND, OR, NOR using NAND gate. 7 M

UNIT-III

5. a) Define decoder. Construct 3x8 decoder using logic gates. 7 M

b) Realize the function
$F(A,B,C,D) = \sum (1,2,3,4,6,7,8,10,12,14,15)$ using
i) 8:1 MUX ii) 4:1 MUX 7 M

OR

6. a) Design 4-bit parallel adder circuit. 7 M

b) Define multiplexer. Construct 4-to-1 multiplexer using logic gates. 7 M

UNIT – IV

7. a) Explain the operation of 4-bit Ring counter with the help of sequential circuit and timing diagram. 7 M

b) Design and implement Mod-9 Synchronous Counter using JK-Flip flop and construct the timing diagram. 7 M

OR

8. a) Design a Mod -11 Ripple counter using T flip flops and explain its operation with the help of the state diagram. 7 M

b) Implement 4-bit Bi-Directional shift register and explain its operation. 7 M

UNIT – V

9. a) With simple examples explain the differences between Mealy and Moore type machines. 7 M

b) Describe the design procedure for synchronous sequential circuits. 7 M

OR

10. a) State the objectives of FSM and Explain Moore state machine with example. 7 M

b) Obtain the state table and state diagram for a sequence detector to recognize the occurrence of sequence bits 110 & 001. 7 M